DEC 1 2 2003
PATENT & TRADEMARK OFFICE

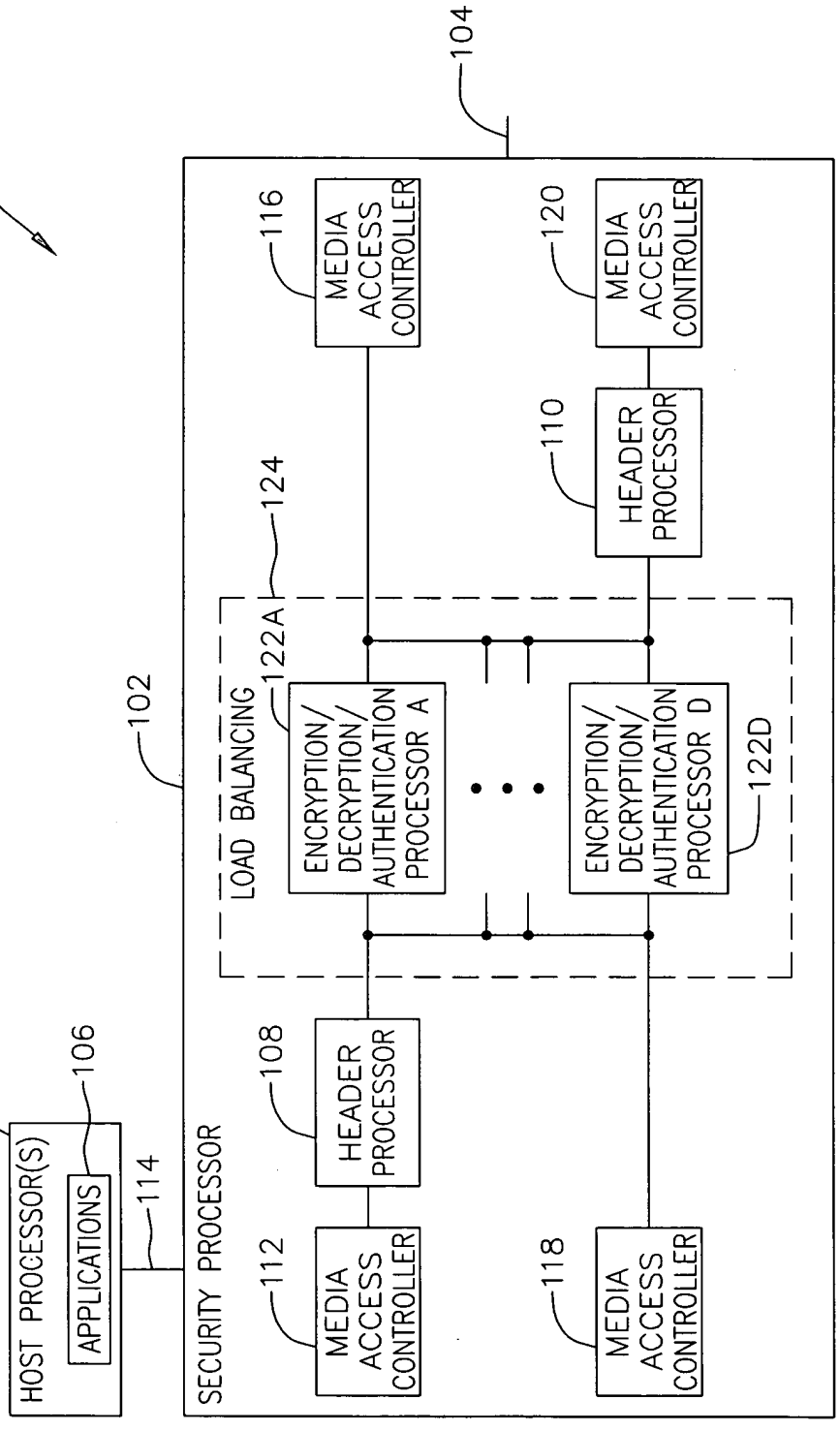


FIG. 1

FIG. 2

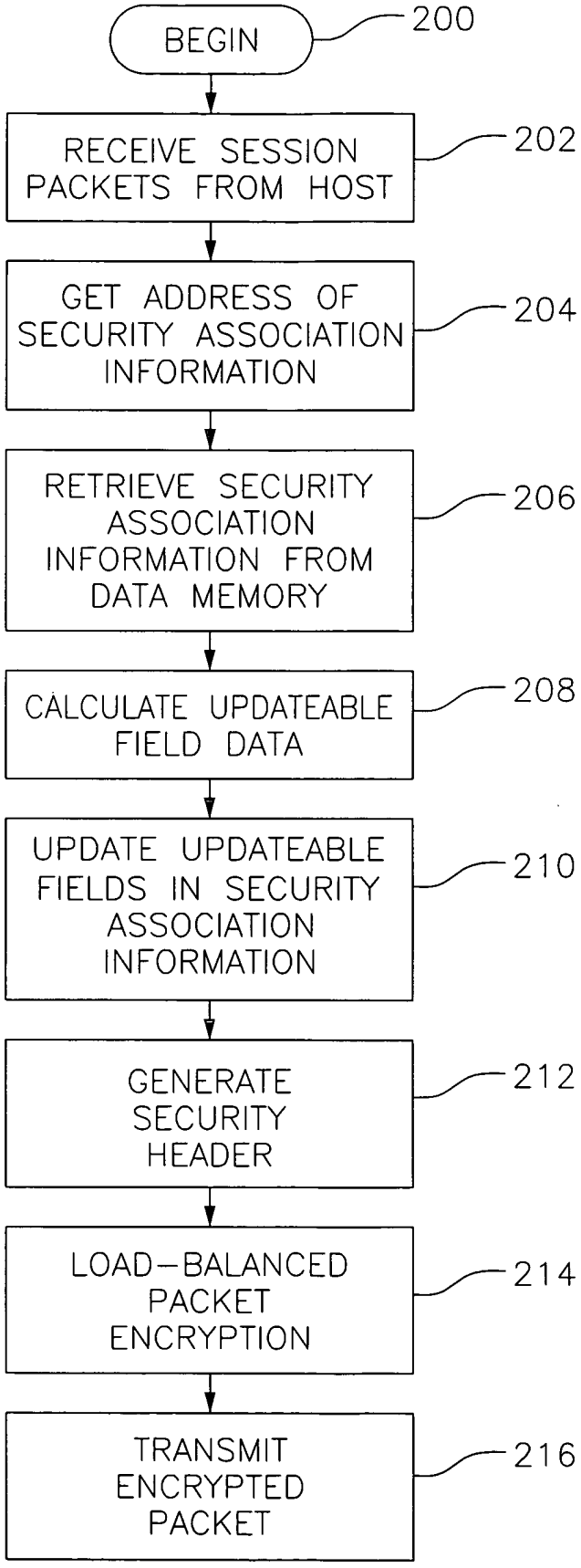
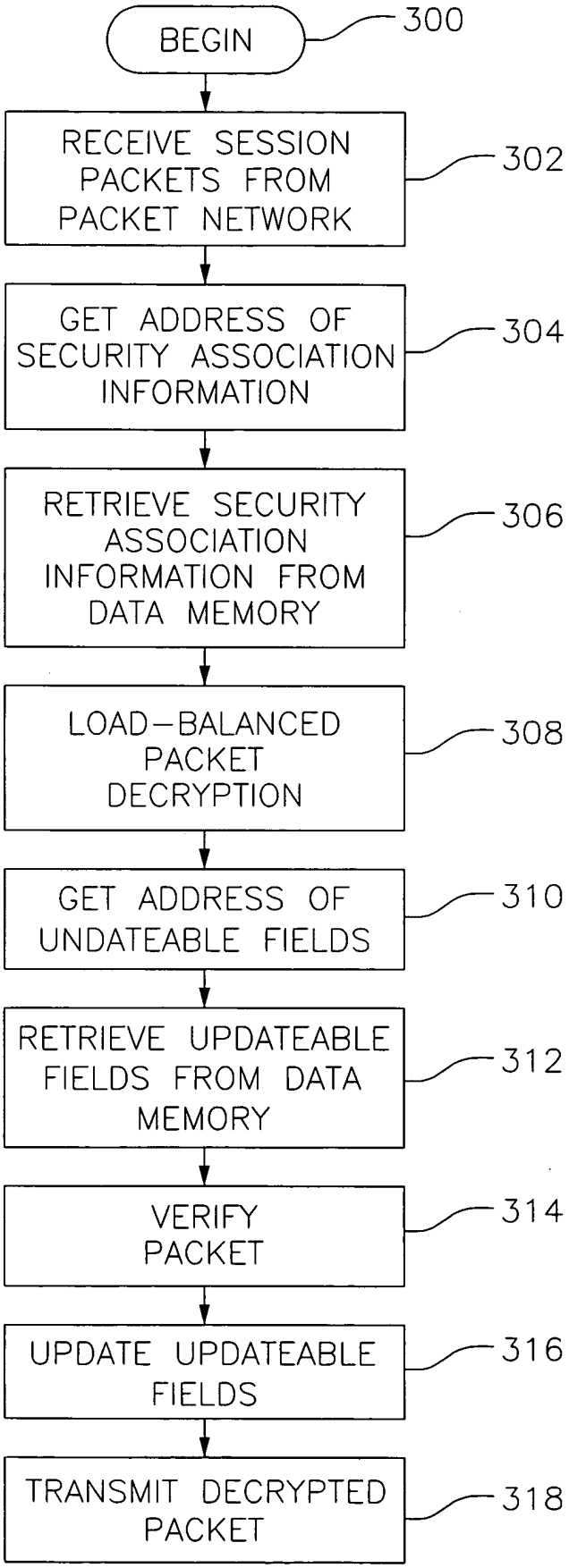

BEGIN
200
RECEIVE SESSION PACKETS FROM HOST
202
GET ADDRESS OF SECURITY ASSOCIATION INFORMATION
204
RETRIEVE SECURITY ASSOCIATION INFORMATION FROM DATA MEMORY
206
CALCULATE UPDATEABLE FIELD DATA
208
UPDATE UPDATEABLE FIELDS IN SECURITY ASSOCIATION INFORMATION
210
GENERATE SECURITY HEADER
212
LOAD-BALANCED PACKET ENCRYPTION
214
TRANSMIT ENCRYPTED PACKET
216

FIG. 3


BEGIN
300
RECEIVE SESSION PACKETS FROM PACKET NETWORK
302
GET ADDRESS OF SECURITY ASSOCIATION INFORMATION
304
RETRIEVE SECURITY ASSOCIATION INFORMATION FROM DATA MEMORY
306
LOAD-BALANCED PACKET DECRYPTION
308
GET ADDRESS OF UNDATEABLE FIELDS
310
RETRIEVE UPDATEABLE FIELDS FROM DATA MEMORY
312
VERIFY PACKET
314
UPDATE UPDATEABLE FIELDS
316
TRANSMIT DECRYPTED PACKET
318

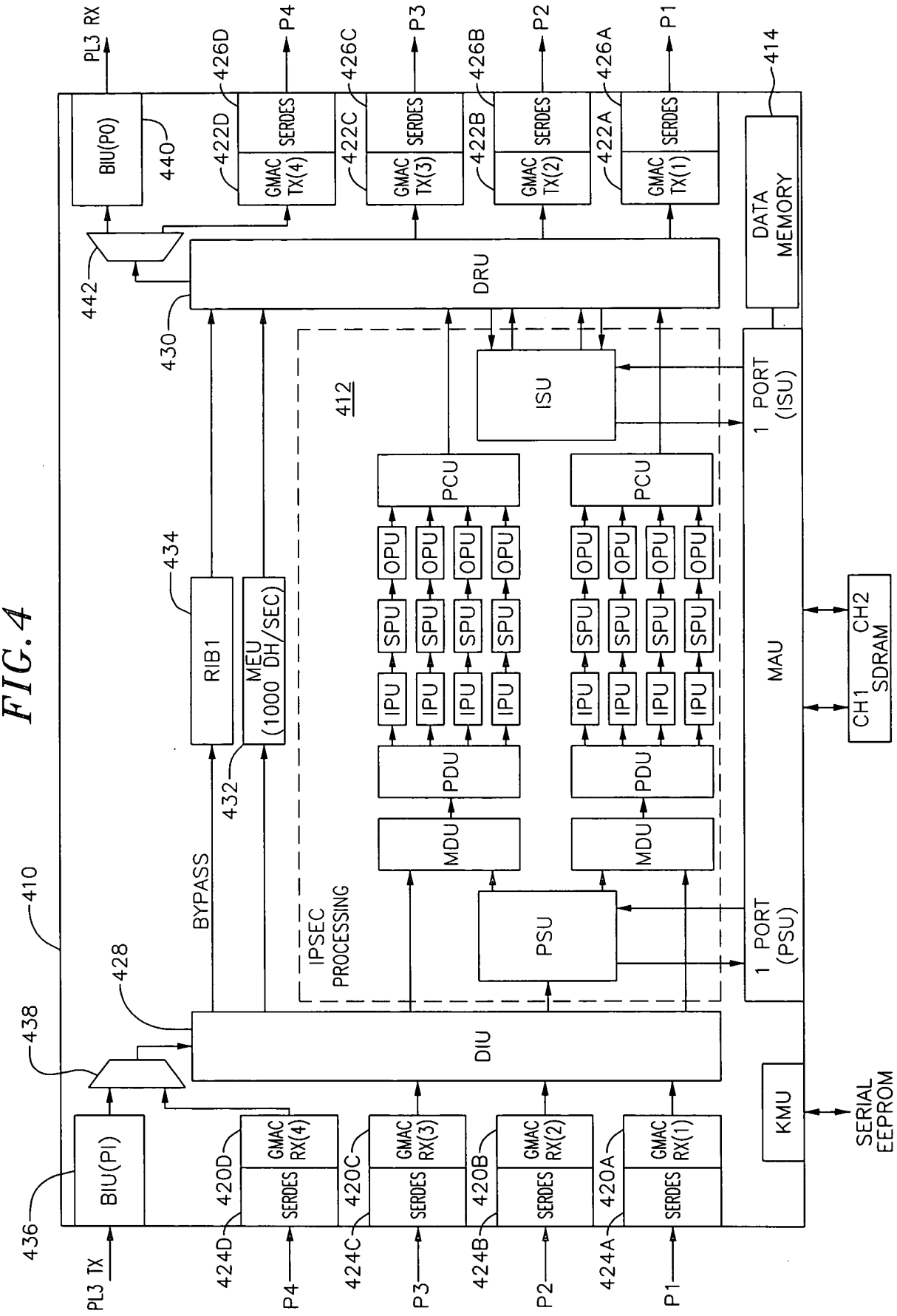

PL3 RX
BIU(P0)
440
426D
422D
GMAC TX(4)
SERDES
P4
426C
422C
GMAC TX(3)
SERDES
P3
426B
422B
GMAC TX(2)
SERDES
P2
426A
422A
GMAC TX(1)
SERDES
P1
414
DATA MEMORY
442
DRU
430
412
ISU
1 PORT (ISU)
PCU
OPU
SPU
IPU
PDU
MDU
PSU
434
RIB1
MEU (1000 DH/SEC)
BYPASS
432
IPSEC PROCESSING
410
428
DIU
MAU
CH1 SDRAM
CH2
438
KMU
SERIAL EEPROM
436
BIU(P1)
420D
GMAC RX(4)
SERDES
420C
GMAC RX(3)
SERDES
420B
GMAC RX(2)
SERDES
420A
GMAC RX(1)
SERDES
424D
424C
424B
424A
PL3 TX
P4
P3
P2
P1

FIG. 4

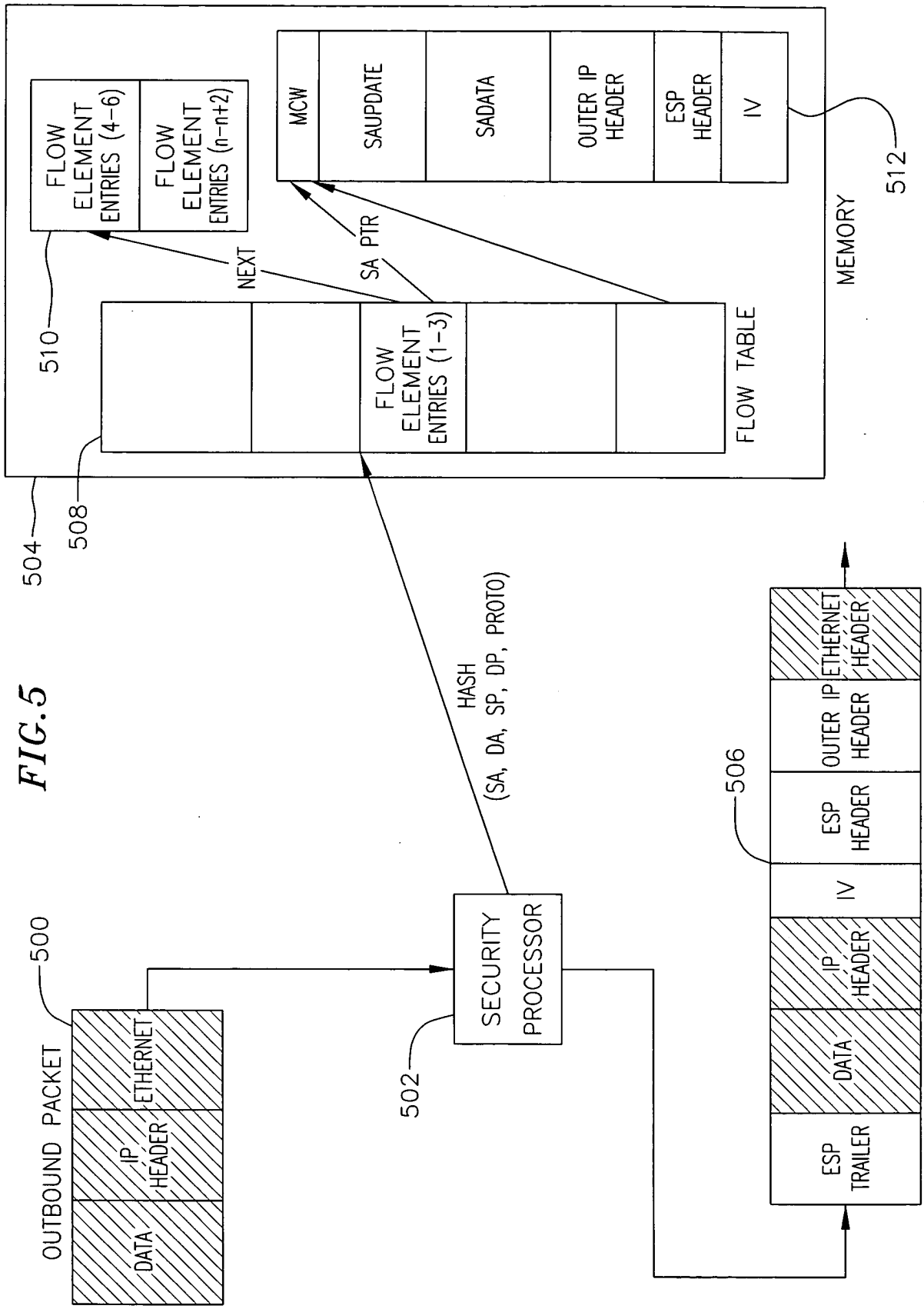

MEMORY
512
MCW
SAUPDATE
SADATA
OUTER IP HEADER
ESP HEADER
IV
FLOW ELEMENT ENTRIES (4-6)
FLOW ELEMENT ENTRIES (n-n+2)
NEXT
SA PTR
510
FLOW ELEMENT ENTRIES (1-3)
FLOW TABLE
504
508
HASH
(SA, DA, SP, DP, PROTO)
OUTBOUND PACKET
500
ETHERNET
IP HEADER
DATA
SECURITY PROCESSOR
502
506
ETHERNET HEADER
OUTER IP HEADER
ESP HEADER
IV
IP HEADER
DATA
ESP TRAILER

FIG. 5

FIG. 6

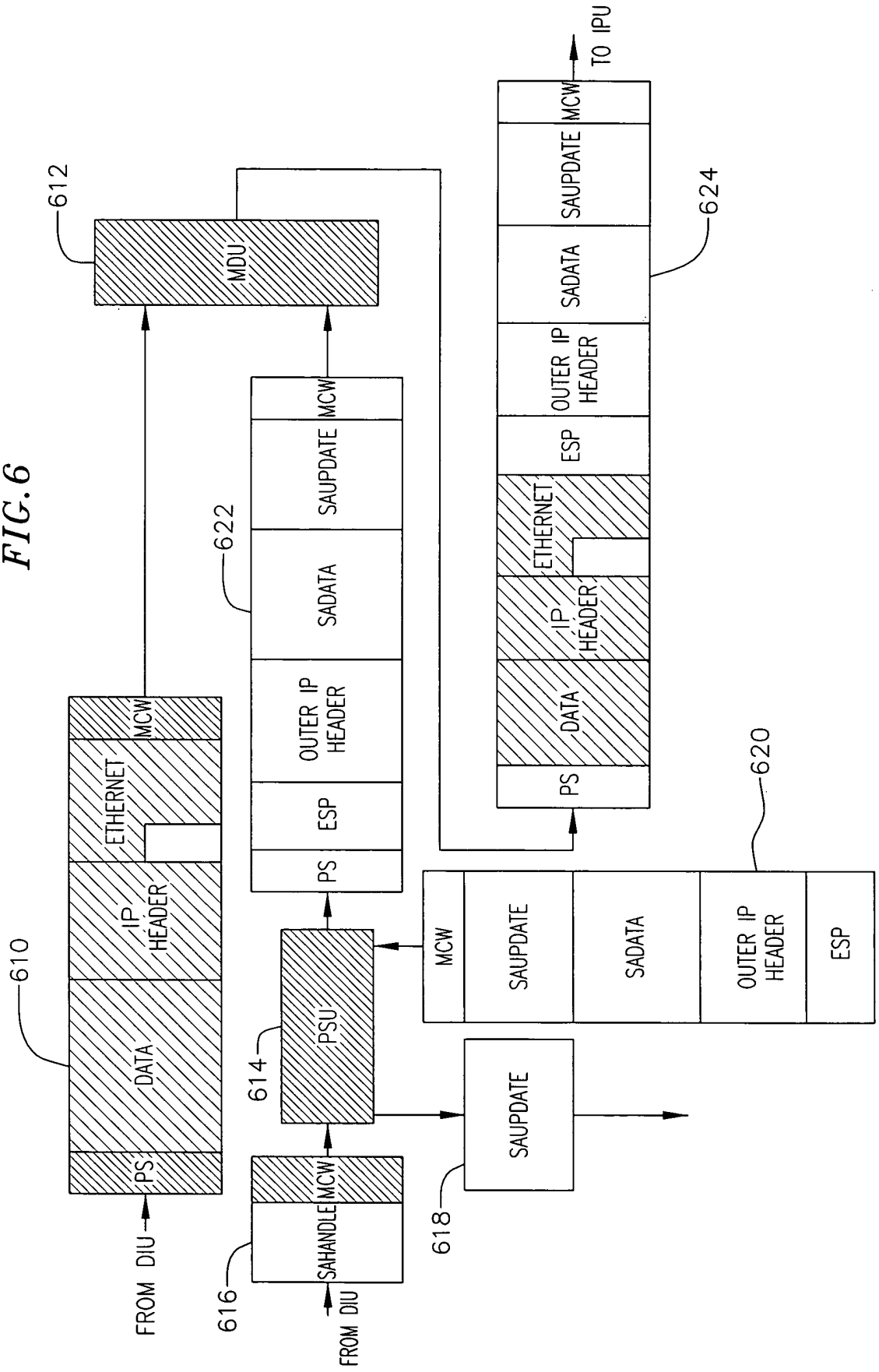

612
MDU
622
PS
ESP
OUTER IP HEADER
SADATA
SAUPDATE
MCW
624
PS
DATA
IP HEADER
ETHERNET
ESP
OUTER IP HEADER
SADATA
SAUPDATE
MCW
TO IPU
610
PS
DATA
IP HEADER
ETHERNET
MCW
614
PSU
616
SAHANDLE
MCW
FROM DIU
FROM DIU
618
SAUPDATE
620
MCW
SAUPDATE
SADATA
OUTER IP HEADER
ESP

FIG. 7

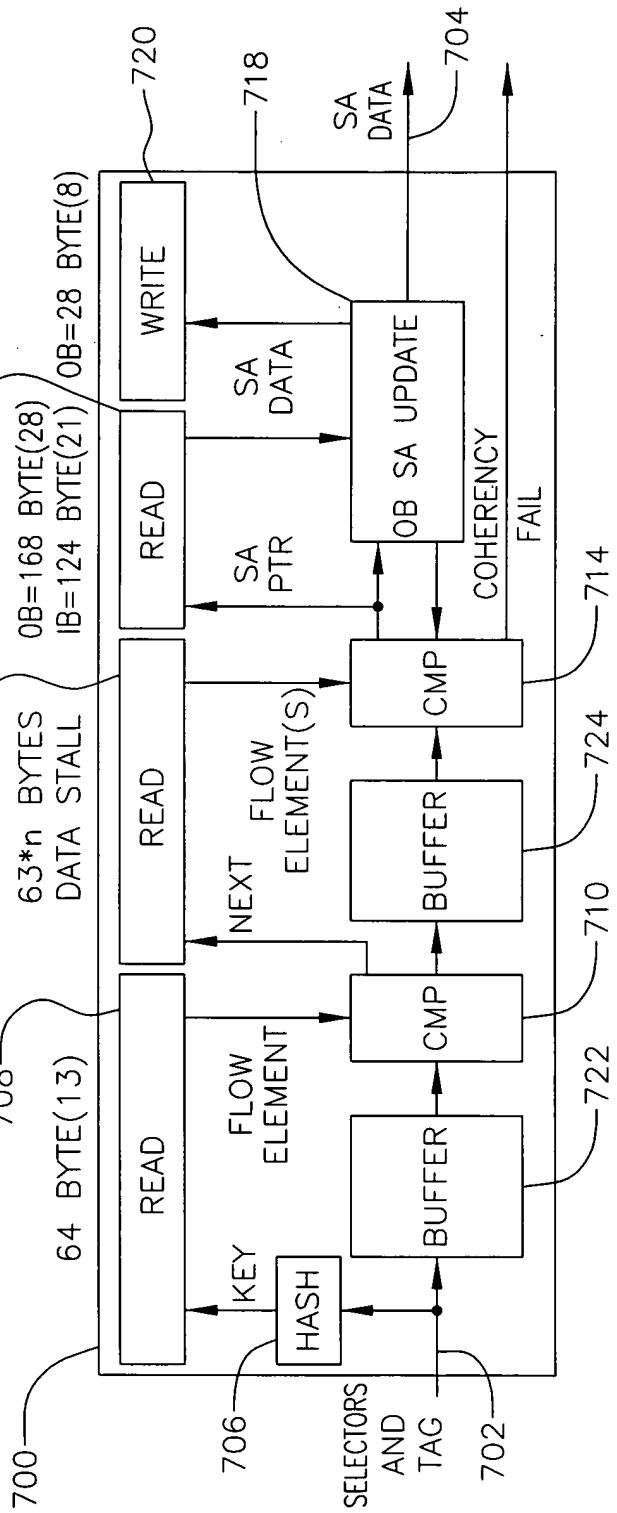
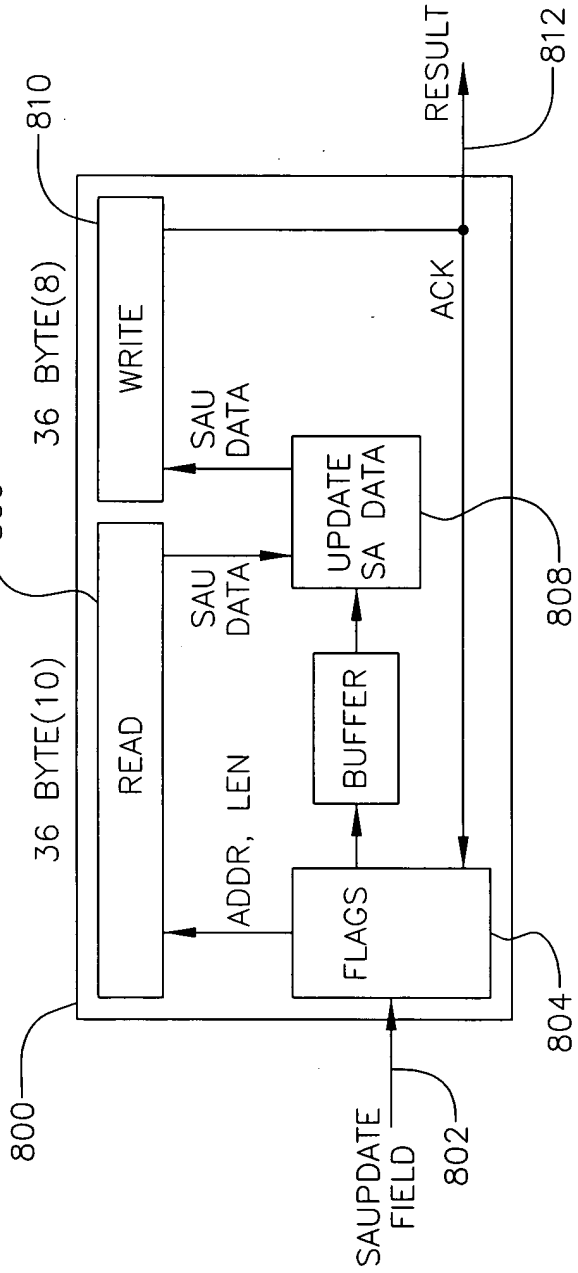

720
718
704
SA DATA
WRITE
READ
READ
READ
OB=28 BYTE(8)
OB=168 BYTE(28)
IB=124 BYTE(21)
63*n BYTES DATA STALL
64 BYTE(13)
SA DATA
SA PTR
NEXT FLOW ELEMENT(S)
FLOW ELEMENT
KEY
HASH
OB SA UPDATE
COHERENCY FAIL
CMP
CMP
BUFFER
BUFFER
716
712
708
714
724
710
722
700
706
SELECTORS AND TAG
702

FIG. 8


800
802
804
806
808
810
812
SAUPDATE FIELD
FLAGS
ADDR, LEN
BUFFER
SAU DATA
UPDATE SA DATA
SAU DATA
ACK
RESULT
36 BYTE(10)
READ
36 BYTE(8)
WRITE

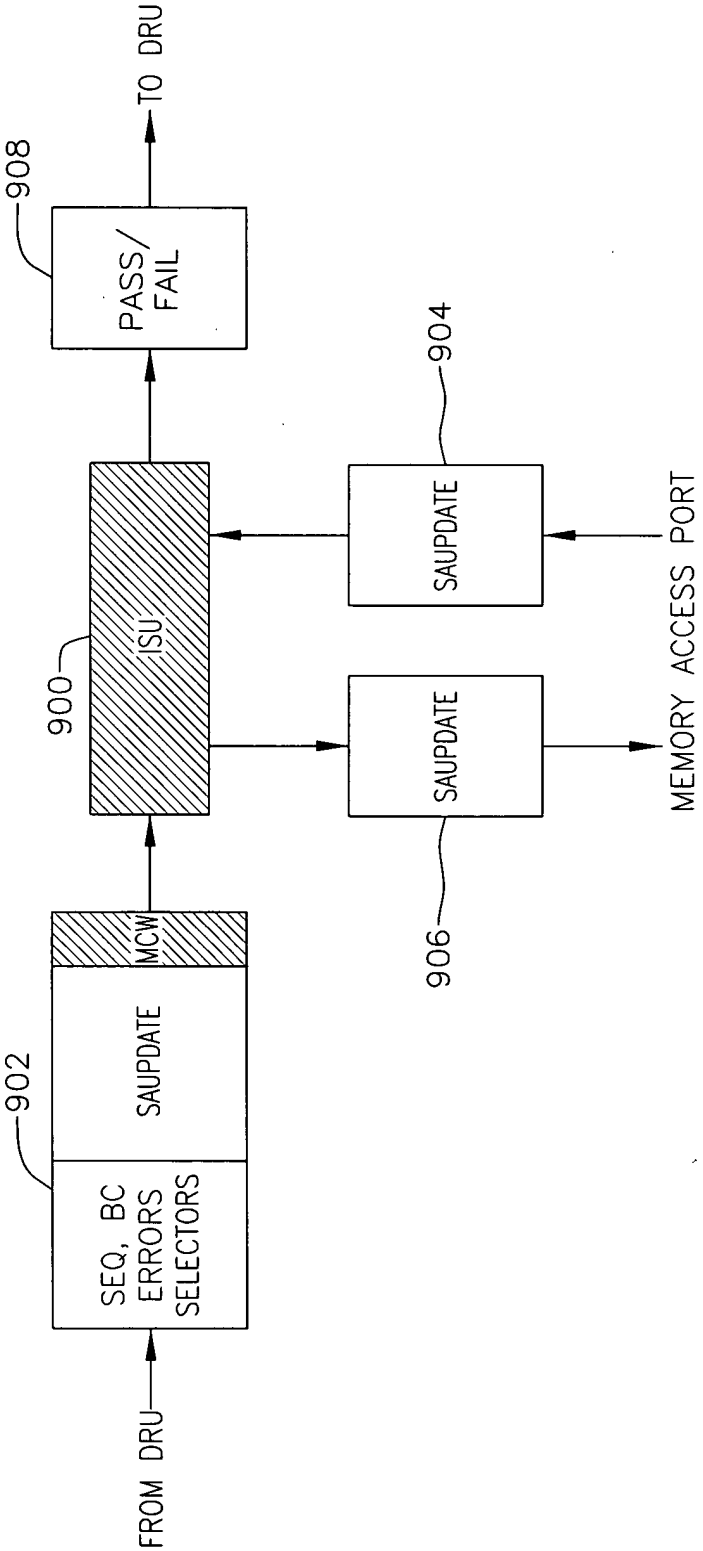

FROM DRU
902
SEQ, BC ERRORS SELECTORS
SAUPDATE
MCW
900
ISU
906
SAUPDATE
904
SAUPDATE
MEMORY ACCESS PORT
908
PASS/ FAIL
TO DRU

FIG. 9

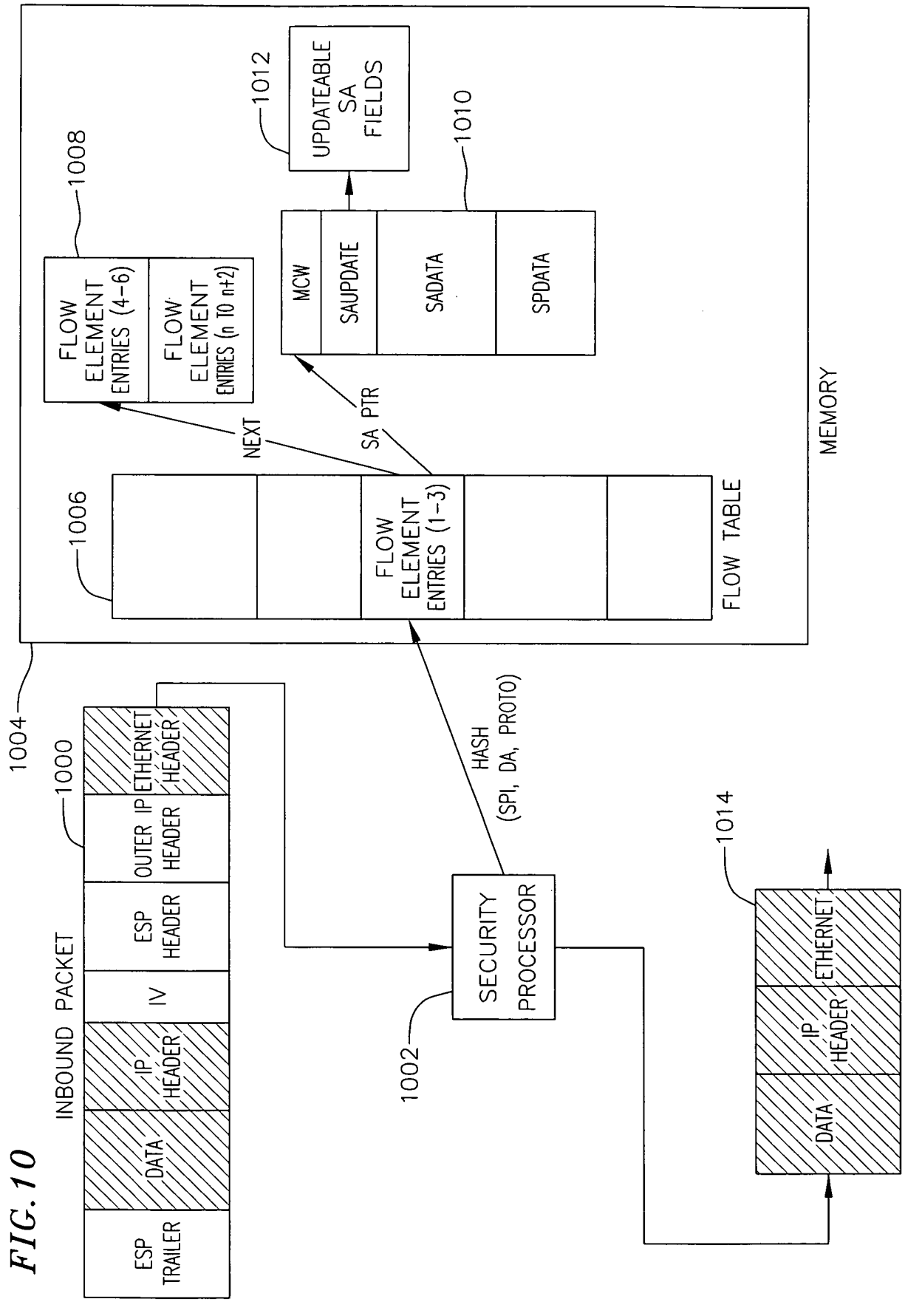
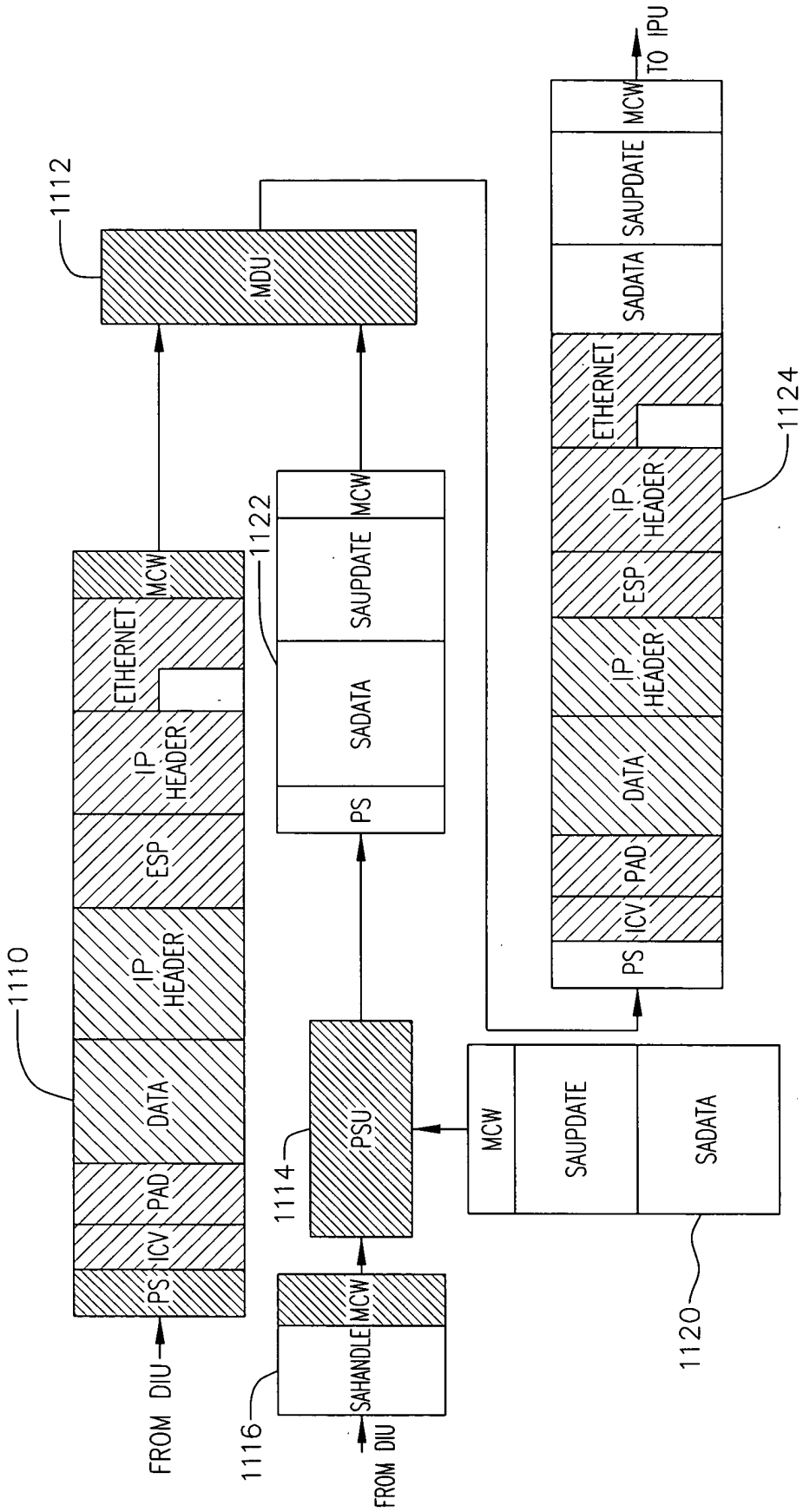

MEMORY
FLOW TABLE
1006
FLOW ELEMENT ENTRIES (1-3)
1008
FLOW ELEMENT ENTRIES (4-6)
FLOW ELEMENT ENTRIES (n TO n+2)
NEXT
SA PTR
1010
MCW
SAUPDATE
SADATA
SPDATA
1012
UPDATEABLE SA FIELDS
1004
1000
INBOUND PACKET
ETHERNET HEADER
OUTER IP HEADER
ESP HEADER
IV
IP HEADER
DATA
ESP TRAILER
HASH (SPI, DA, PROTO)
1002
SECURITY PROCESSOR
1014
ETHERNET
IP HEADER
DATA

FIG. 10

FIG. 11


1112
MDU
1122
MCW
SAUPDATE
SADATA
PS
1110
MCW
ETHERNET
IP HEADER
ESP
IP HEADER
DATA
PAD
ICV
PS
1114
PSU
MCW
SAUPDATE
SADATA
1120
1124
MCW
SAUPDATE
SADATA
ETHERNET
IP HEADER
ESP
IP HEADER
DATA
PAD
ICV
PS
TO IPU
FROM DIU
1116
SAHANDLE
MCW
FROM DIU